IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant	:	Christopher P. Duff	
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Examiner	:	Leon Flores	
Docket No.	:	10040178-01	

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PRE-APPEAL BRIEF

This Pre-Appeal Brief is submitted with a Notice of Appeal, and in response to the Final Office Action mailed July 10, 2008.

Claims 1-13, 16, 17, 22-31, 34, 35, 39-47 and 50 stand rejected under 35 USC 103(a) as being unpatentable over Jeong et al. (US 6,229,859 B1; hereinafter "Jeong") in view of Kirisawa (US 5,847,619). With respect to claim 1, the Examiner admits that Jeong does not teach "displaying. . .at least some of the digital interface symbol information with a representation of the set of data samples of the at least one analog signal in a correlated fashion." This, the Examiner asserts, is taught by Kirisawa. More specifically, the Examiner indicates:

> . . .(See figs. 1 & 3 & col. 1, lines 30-34, col. 3, lines 25-45, col. 4, lines 57-63) Kirisawa discloses a system a calibration system comprising of a quadrature signal generator, quadrature phase modulator, and a spectrum analyzer for displaying the output from the phase modulator.
>
> Taking the combined teachings of Jeong and Kirisawa as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Jeong, in the manner as claimed and as taught by Kirisawa, for the benefit of analyzing the phase modulated signal.

4/15/2008 Final Office Action, p. 4, sec. 3.

Applicant respectfully disagrees. Some of the excerpts of Kirisawa cited by the Examiner state:

> Referring to FIG. 3, a calibration system according to a first embodiment of the present invention is used for a quadrature phase modulator 10 which includes a local oscillator 11 for generating a carrier wave, a first mixer 12 for mixing I-signal with the carrier wave, a second mixer 13 for mixing Q-signal with a phase-corrected carrier wave obtained by shifting the carrier wave by 90° in phase, a 90° phase shifter 14 for phase-shifting carrier signal for the mixer 13, and a hybrid (H) block (or combiner) 15 for synthesizing the outputs of the mixers 12 and 13.
>
> The calibration system comprises a sine-wave quadrature signal generator 20 for generating sine-wave quadrature signals having a phase difference of 90° therebetween, an adjusting block 30 integrated to the quadrature phase modulator 10 for adjusting the phase difference and amplitude difference between the sine-wave quadrature signals to supply the adjusted quadrature signals to the mixers 12 and 13 of the quadrature phase modulator 10, and a frequency spectrum analyzer for receiving the output of the quadrature phase modulator 10 to observe the frequency spectrum in the output of the quadrature phase modulator 10.
>
> Col. 3, lines 25-45.
>
> The spectrum analyzer 40 of the calibration system displays thereon the output of the quadrature phase modulator 10 in terms of frequency spectrum. While observing the frequency spectrum analyzer 40 or monitoring the output of the quadrature phase modulator, the quadrature phase modulator is calibrated. Calibration by the calibration system of the present embodiment will be described hereinafter.
>
> Col. 4, lines 57-63.

Of note, neither of the above excerpts says anything about displaying "***digital interface symbol information***" or displaying such digital interface symbol information "with a representation of the set of data samples of the at least one analog signal ***in a correlated fashion***". Rather, the above excerpts only indicate that "the output of the quadrature phase modulator 10 in terms of frequency spectrum" is displayed (col. 4, lines 57-63).

Kirisawa provides examples of the spectrum analyzer 40's display in FIGS. 7A-7D (col. 4, line 64 - col. 5, line 5). In these displays, it is noted that there is no display of

"digital interface symbol information". In fact, there is no display of any digital information at all. Although Kirisawa does illustrate waveforms containing at least some digital information in FIGS. 5A and 5B (although not digital interface symbol information), it is noted that the waveforms shown in FIGS. 5A and 5B are representative of waveforms generated by the sin ROM 23 and cos ROM 24 of the quadrature signal generator 20 (see, FIGS. 3 & 4; and col. 3, lines 60-65). The waveforms shown in FIGS. 5A and 5B are not displayed on the spectrum analyzer 40, and the waveforms shown in FIGS. 5A and 5B are not correlated with any "digital interface symbol information".

For the reasons given above, applicant does not believe that Kirisawa teaches "displaying. . .at least some of the digital interface symbol information with a representation of the set of data samples of the at least one analog signal in a correlated fashion". In his Advisory Action, the Examiner disagrees and asserts that:

> . . .Kirisawa teaches a calibration system comprised of quadrature phase modulator which includes a local oscillator for generating a carrier wave, a first mixer for mixing I-signal (digital data) with the carrier signal, a second mixer for mixing Q-signal (digital data) with the carrier wave, and a hybrid block for combining the output of the two mixers. One skilled in the art would know that these signals are further displayed by the spectrum analyzer. (See fig. 3 & col. 4, lines 57-61) As you can see, the concept of displaying digital data and an analog signal in a correlated fashion is not novel.

However, applicant believes that the Examiner's above conclusion is wholly unsupported by Kirisawa. Col. 4, lines 57-61 (cited by the Examiner) are followed by a discussion of FIGS. 7A-7D, which illustrate what is *actually shown* by Kirisawa's spectrum analyzer. FIGS. 7A-7D and their related description clearly indicate that Kirisawa's spectrum analyzer does not display "digital interface symbol information with a representation of the set of data samples of. . .at least one analog signal in a correlated fashion".

Because of the above-noted deficiencies of Jeong and Kirisawa, claim 1 is believed to be allowable over their combined teachings.

Claims 2-13, 16, 17, 22-31, 34, 35, 39-47 and 50 are believed to be allowable, at least, because they depend from claim 1, or for reasons similar to why claim 1 is believed to be allowable.

Claims 14, 15, 18-20, 32, 33, 36-38, 48, 49 and 51-53 stand rejected under 35 USC 103(a) as being unpatentable over Jeong in view of Kirisawa and Sajdak et al. (US 6,570,592 B1; hereinafter "Sajdak"). These claims are believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable, and because Sajdak fails to disclose that which is missing from Jeong and Voutilainen (see, e.g., Section 1 of these Remarks/Arguments).

Claims 1, 22 and 39 also stand rejected under 35 USC 103(a) as being unpatentable over Jeong in view of Iida (US 7,236,513 B2). With respect to claim 1, the Examiner once again admits that Jeong fails to teach "displaying. . .at least some of the digital interface symbol information with a representation of the at least one analog signal in a correlated fashion." However, the Examiner asserts that Iida teaches this in FIGS. 2A-N & col. 6, line 39 - col. 7, line 12. Applicant respectfully disagrees.

What is shown in Iida's FIGS. 2A-N are signals appearing at various different nodes of the transmitter 100 shown in FIG. 1. Iida contains absolutely no teaching that any of the signals shown in FIGS. 2A-N are actually displayed in a correlated fashion. Iida certainly does not indicate that "digital interface symbol information [captured from a set of data samples for at least one analog signal is displayed] with a representation of the set of data samples of the at least one analog signal in a correlated fashion", as is recited in applicant's claim 1.

Because of the above-noted deficiencies of Jeong and Kirisawa, claim 1 is believed to be allowable over their combined teachings.

In response to the above arguments, the Examiner disagrees and indicates that:

> . . .Iida does teach displaying at least some of the digital interface symbol information (figs 2D & E "I & Q signals) with a representation of the at least one

analog signal (figs. 2H & I "carrier signals") in a correlated fashion. (figs 2J-M "I & Q signals modulating the carrier signal")

7/10/2008 Final Office Action, p. 4.

However, applicant believes the Examiner's references to different figures showing different things is, in and of itself, illustrative of the fact that Iida does not teach ""displaying. . .at least some of the digital interface symbol information with a representation of the at least one analog signal ***in a correlated fashion***."

Claims 22 and 39 are believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

In light of the remarks provided herein, and the noted deficiencies of the references cited by the Examiner, applicant believes the Examiner has committed clear error, in that the Examiner has not made a prima facie case for rejecting any of applicant's claims. As a result, applicant respectfully requests the issuance of a Notice of Allowance.

Respectfully submitted,
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